7. The field effect transistor of claim 5, wherein:

the lightly n-doped body region is disposed between the respective source region, the gate insulator region, and the drain region proximate the trench gate region; and

the heavily n-doped body region is disposed between the drain region, the lightly n-doped body region, the respective source region, and the source metal contact.

8. The field effect transistor of claim 1, further comprising a Schottky junction disposed at the top surface where the source metal contact is physical contact with the portion of the drain region.

9. The field effect transistor of claim 1, wherein said pair of source regions are formed as substantially parallel elongated structures.

10. A field effect transistor comprising:

a first and second trench gate regions extending into a semiconductor substrate for a first predetermined depth;

a first source region disposed in the semiconductor substrate and proximate the first trench gate region;

a second source region disposed in the semiconductor substrate and proximate the second trench gate region;

a first lightly-doped body region disposed below said first source region proximate said first trench gate region and extending into the semiconductor substrate for a depth that is less than the first predetermined depth;

a second lightly-doped body region disposed below said second source region proximate said second trench gate region and extending into the semiconductor substrate for a depth that is less than the first predetermined depth;

a third heavily-doped body region disposed in the semiconductor substrate and adjacent said first source region and above said first lightly-doped body region;

a fourth heavily-doped body region disposed in the semiconductor substrate and adjacent said second source region and above said second lightly-doped body region;

a drain region disposed in the semiconductor substrate and between said first and second lightly-doped body regions and said third and fourth heavily-doped body regions and between said first and second gate regions, wherein said first lightly-doped body region and said third heavily-doped body region are disposed between said drain region and said first source region and wherein said second lightly-doped body region and said fourth heavily-doped body region are disposed between said drain region and said second source region;

a source contact disposed on a top surface of the semiconductor substrate and-in physical contact with said first and second source regions, said third and fourth heavily-doped body regions and a portion of said drain region disposed between said first and second trench gate regions;

a first gate insulator region insulating said first trench gate region from said first source region, said first lightly-doped body region, said drain region, and said source contact; and

a second gate insulator region insulating said second trench gate region and said second source region, said second lightly-doped body region, said drain region, and said source contact.

11. The field effect transistor of claim 10, wherein:

said first and second source regions comprise an n-doped semiconductor;

said drain region comprises an n-doped semiconductor; and

said first and second lightly-doped body regions comprise a p-doped semiconductor.

12. The field effect transistor of claim 11, wherein said drain region comprises: a heavily n-doped portion; and

a lightly n-doped portion disposed between said heavily n-doped portion and said first and second lightly-doped body regions, said third and fourth heavily-doped body regions, and said source contact.

13. The field effect transistor of claim 11, wherein:

said first lightly-doped body region comprises a lightly p-doped portion disposed between said first source region and said drain region proximate said gate region;

said third heavily-doped body region comprises a heavily p-doped portion disposed proximate said drain region and said source contact;

said second lightly-doped body region comprises a lightly p-doped portion disposed between said second source region and said drain region proximate said gate region; and

said fourth heavily-doped body region comprises a heavily p-doped portion disposed proximate said drain region and said source contact.

14. The field effect transistor of claim 11, wherein:

said first and second source regions comprise a p-doped semiconductor;

said drain region comprises a p-doped semiconductor; and

said first and second lightly-doped body regions comprise an n-doped semiconductor.

15. The field effect transistor of claim 14, wherein said drain region comprises:

a heavily p-doped portion; and

a lightly p-doped portion disposed between said heavily p-doped portion and said first and second lightly-doped body regions, said third and fourth heavily-doped body regions, and said source contact.

16. The field effect transistor of claim 14, wherein:

said first lightly-doped body region comprises a lightly n-doped portion disposed between said first source region and said drain region proximate said first gate region;

said third heavily-doped body region comprises a heavily n-doped portion disposed proximate said source contact;

said second lightly-doped body region comprises a lightly n-doped portion disposed between said second source region and said drain region proximate said second gate region; and

said fourth heavily-doped body region comprises a heavily n-doped portion disposed proximate said source contact.

17. The field effect transistor of claim 10, further comprising a Schottky junction disposed at an interface between said source contact and said portion of said drain region proximate said first and second lightly-doped body regions.

18. The field effect transistor of claim 10, wherein said first and said second gate regions are formed as substantially parallel elongated structures.

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